


INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Complete if Known			
		Application Number			
		Filing Date			
		First Named Inventor	Marius K. Orlowski		
		Group Art Unit			
		Examiner Name			
Sheet 1	1	of	1	Attorney Docket Number	SC13240TP

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number -Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
<i>PO</i>	AA	US -2003/0201505 A1	10-30-2003	KURATA	
	AB	US -6,646,326 B1	11-11-2003	KIM	
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Examine r Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ² (if known)				
	AF	PT WO 00/34984	06-15-2000	CHU		

NON PATENT LITERATURE DOCUMENTS				T ²
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		
<i>PO</i>	AG	PIDIN et al., "A Notched Metal Gate MOSFET for sub-0.1 μ m Operation," IEEE, pp. 29.1.1 – 29.1.4 (2000).		
	AH	GHANI et al., "100 nm Gate Length High Performance/Low Power CMOS Transistor Structure," IEEE, IEDM 99-415, pp. 17.1.1 – 17.1.4 (1999).		
	AI	SKOTNICKI et al., "Well-controlled, Selectively Under-Etched Si/SiGe gates for RF and High Performance CMOS," IEEE 2000 SYMPOSIUM ON VLSI TECHNOLOGY DIGEST OF TECHNICAL PAPERS, pp. 156-157.		
	AJ	NAKAI et al., "A 100 nm CMOS Technology with Sidewall Notched 40 nm Transistors and SiC-Capped Cu/VLK Interconnects for High Performance Microprocessor Applications," IEEE 2002 SYMPOSIUM ON VLSI TECHNOLOGY DIGEST OF TECHNICAL PAPERS, pp. 66-67.		
	AK	WU et al., "Notched Sub-100 nm Gate MOSFETs for Analog Applications," IEEE 2001 SOLID-STATE AND INTEGRATED-CIRCUIT TECHNOLOGY PROCEEDINGS, pp. 539-542.		
<i>PO</i>	AL	PIDIN et al., "Experimental and Simulation Study on Sub-50 nm CMOS Design," 2001 SYMPOSIUM ON VLSI TECHNOLOGY DIGEST OF TECHNICAL PAPERS, pp. 35-36.		

Examiner Signature	<i>Richard J. [Signature]</i>	Date Considered	09/28/05
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¹ Unique citation designation number. ² See Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English Language Translation is attached.

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